

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
3	10/6	Parallel Computer: The state of computing	I	CR		
3	11/6	Computer development milestones, elements of modern computers	I	CR		
3	13/6	Evolution of computer architecture System attributes to performance	I	CR		
4	14/6	Multiprocessors & multicomputers shared memory multiprocessors	I	CR		
3	17/6	Distributed memory multiprocessors A taxonomy of multicomputers	I	CR		
3	18/6	Multivector & SIMD Computers Vector Super Computer	I	CR		
3	20/6	SIMD Super computers.	I	CR		
			<u>II</u>			
4	24/6	Memory Hierarchy Design	II	CR		
3	24/6	Basic memory hierarchy	II	CR		
3	25/6	Optimization of Cache performance Small and simple first level caches to reduce hit time	II	CR		
3	27/6	Way Prediction to reduce hit time	II	CR		
4	28/6	Pipelined Cache Access to increase Cache Bandwidth	II	CR		
3	1/7	Non blocking caches to increase Cache Bandwidth	II	CR		
3	2/7	Virtual memory & Virtual machines	II	CR		
3	4/7	Protection via virtual memory	II	CR		
4	5/7	Protection via virtual machines	II	CR		

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3	8/7	Design space of processors	<u>II</u>	CR		
3	9/7	Instruction set architectures	<u>III</u>	CR		
3	11/7	characteristics of typical CISC & RISC architectures	<u>III</u>	CR		
4	12/7	Hierarchical memory technology	<u>III</u>	CR		
3	15/7	Inclusion	<u>III</u>	CR		
3	16/7	Coherence & locality.	<u>III</u>	CR		
			<u>IV</u>			
3	18/7	linear & non linear Pipeline processors	<u>IV</u>	CR		
4	19/7	Asynchronous & Synchronous models	<u>IV</u>	CR		
3	22/7	Clocking and Timing control	<u>IV</u>	CR		
3	23/7	Speedup, Efficiency & Throughput.	<u>IV</u>	CR		
3	25/7	Nonlinear pipeline processors.	<u>IV</u>	CR		
4	26/7	Reservation and Latency analysis problems	<u>IV</u>	CR		
3	29/7	Collision free Scheduling problems	<u>IV</u>	CR		
3	29/7	Instruction Execution Phases -	<u>IV</u>	CR		
3	30/7	Multiprocessors & Multivector Computers	<u>V</u>	CR		
3	30/7	Hierarchical Bus Systems	<u>V</u>	CR		
3	1/8	Crossbar Switch and multipoint memory	<u>V</u>	CR		

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4	2/8	multistage and Combining networks	<u>IV</u>	CL		
3	12/8	Routing, the Hot Spot Problem.	<u>IV</u>	CL		
3	13/8	Application & Drambanks	<u>V</u>	CL		
3	15/8	Multistage n/w's in Real Systems	<u>V</u>	CL		
4	16/8	Multivector Computers	<u>V</u>	CL		
3	19/8	Vector Processing Principles Vector Instruction Types	<u>V</u>	CL		
3	20/8	Vector Access memory Schemes.	<u>V</u>	CL		
3	22/8	Cray Ymp multivector multiprocessors.	<u>V</u>	CL		
3	23/8	Cray Ymp 816 System Organization	<u>V</u>	CL		
3	25/8	Multistage Crossbar n/w in the Cray Ymp 816	<u>V</u>	CL		
4	26/8	Cache Coherence and message passing mechanisms	<u>VI</u>	CL		
3	29/8	Cache Coherence problem	<u>VI</u>	CL		
3	30/8	Two protocol approaches	<u>VI</u>	CL		
3	2/9	Snoopy Bus protocols.	<u>VI</u>	CL		
3	3/9	Directory based protocols.	<u>VI</u>	CL		
3	5/9	message passing mechanisms	<u>VI</u>	CL		
3	6/9	Routing Schemes	<u>VI</u>	CL		
3	10/9	Deadlock Virtual channels.	<u>VI</u>	CL		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
3	12/9	Flow control strategies channels	<u>VI</u>	CR		
4	13/9	Multicast Routing Algorithms	<u>VI</u>	CR		
3	16/9	VSIMD & MIMD	<u>VII</u>	CR		
3	17/9	Computer Organizations	<u>VII</u>	CR		
3	19/9	Implementation models	<u>VII</u>	CR		
4	20/9	The cm-2 Architecture	<u>VII</u>	CR		
3	23/9	A Synchronized mimd machine	<u>VII</u>	CR		
3	24/9	Control Processors	<u>VII</u>	CR		
3	26/9	Processing nodes	<u>VII</u>	CR		
4	27/9	Inter processor Commu- cation	<u>VII</u>	CR		
4	29/9	Trends in Parallel	<u>VIII</u>	CR		
		Systems	<u>VIII</u>	CR		
3	30/9	Forms of Parallelism	<u>VIII</u>	CR		
3	1/10	Structural Parallelism	<u>VIII</u>	CR		
3	1/10	Instruction level Parallelism.	<u>VIII</u>	CR		
			<u>VIII</u>	CR		

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